60ns, 35μA, RRI, Push-Pull Output Comparators

Features

- Low Propagation Delay: 60 ns
- Low Quiescent Current: 35μA per Channel
- Low Input Offset Voltage: 1 mV
- Supply Operation From: 1.8V ~ 5.5V
- Rail-to-Rail Inputs
- Push-Pull Outputs
- Internal Hysteresis for Noise Immunity
- Input Bias Current: 1.0 pA Typical
- No Phase Inversion for Overdrive Inputs
- Extended Temperature Ranges
  From -40°C to +125°C
- Small Packaging：MSOP8 and SOP-8

Applications

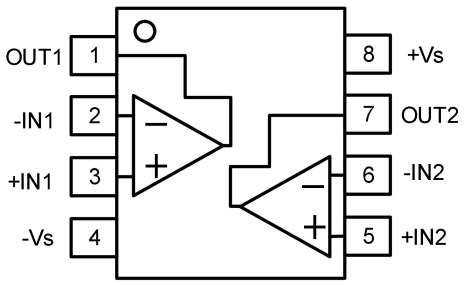
- Inspection Equipment
- Threshold Detectors/Discriminators
- Peak and Zero-crossing detectors
- Logic Level Shifting or Translation
- Portable Equipment
- Sensor Conditioning
- High-Speed Sampling Systems
- Battery Powered Electronics
- IR Receivers
- Window Comparators

General Description

The COS3202 is a dual-channel low-power comparator which features high speed response time with rail-to-rail inputs. It consumes only 35μA per Channel while achieving a 60ns propagation delay. The operating voltage ranges from 1.8 V to 5.5 V. A 1.2mV internal hysteresis is built in to improved noise immunity.

The COS3202 has push-pull output stages capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load. The COS3202 is available in small 8-pin MSOP-8 and SOP-8 packages.

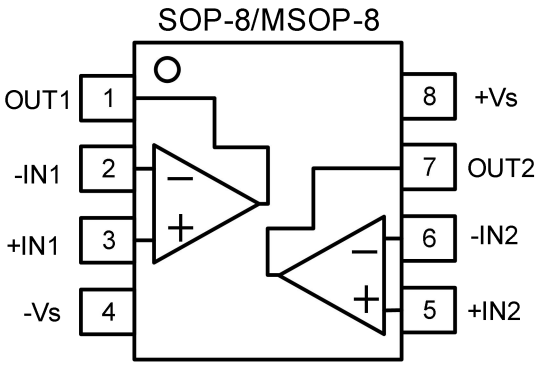
SOP-8/MSOP-8



COS3202

Rev1.0

1. Pin Configuration and Functions



COS3202

Pin Functions

PIN No.	Name	Type	Description
1	OUT1	O	Output, Comparator1
2	-IN1	I	Negative input, Comparator1
3	+IN1	I	Positive input, Comparator1
4	-Vs	P	Negative power supply or ground
5	+IN2	I	Positive input, Comparator2
6	-IN2	I	Negative input, Comparator2
7	OUT2	O	Output, Comparator2
8	+Vs	P	Positive power supply

2. Package and Ordering Information

Model	Channel	Order Number	Package	Package Option	Marking Information
COS3202	2	COS3202SR	SOP-8	Tape and Reel, 4000	COS3202
		COS3202MR	MSOP-8	Tape and Reel, 3000	COS3202

3. Product Specification

3.1 Absolute Maximum Ratings (1)

Parameter	Rating	Units
Power Supply: +Vs to -Vs	6	V
Input Voltage	-Vs -0.5V to +Vs + 0.5V	V
Input Current (2)	±10	mA
Output Short Circuit Current	±70	mA
Storage Temperature Range	-65 to 150	°C
Junction Temperature	150	°C
Operating Temperature Range	-40 to 125	°C
ESD Susceptibility, HBM	3000	V

(1) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

3.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance, $R_{\theta JA}$ (Juntion-to-ambient)	206 (MSOP8) 155 (SOP8)	°C/W

3.3 Recommended Operating Conditions

Parameter	Rating	Unit
DC Supply Voltage	1.8 (±0.9) ~ 5.5 (±2.75)	V
Input Common-mode Voltage Range	-Vs ~ +Vs	V
Operating Ambient Temperature	-40 ~ +125	°C

3.4 Electrical Characteristics

(V_S = 5V, C_L=15pF, T_A=+25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}			1.0	5.0	mV
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40 to 125°C		2	10	µV/°C
Input Hysteresis	V_{HYS}			1.2		mV
Input Bias Current	I_B			1.0	10	pA
Input Offset Current	I_{OS}			1.0	10	pA
Common-Mode Voltage Range	V_{CM}	-40 to 125°C	-0.2		Vs+0.2	V
Common-Mode Rejection Ratio	CMRR	-0.2 V < V_{CM} < 5.2 V	60	75		dB
Output Characteristics						
Voltage Output Swing from Lower Rail	V_{OL}	I_{SINK}=4mA		154		mV
Voltage Output Swing from Upper Rail	V_{OH}	I_{SOURCE}=4mA		150		mV
Short-Circuit Current	I_{SR}	Sourcing		58		mA
	I_{SK}	Sinking		59		mA
Power Supply						
Operating Voltage Range	V_S		1.8		5.5	V
Power Supply Rejection Ratio	PSRR	V_S = +2.5V to +5.5V	70	90		dB
Quiescent Current (per Channel)	I_Q	V_S = +5.0V		35	45	µA
		-40 to 125°C			50	µA
Switching Characteristics						
Propagation Delay Time, High to Low	t_{PHL}	V_{OD} = 100mV		60	75	ns
Propagation Delay Time, Low to High	t_{PLH}	V_{OD} = 100mV		60	75	ns
Rise Time	t_R	10% to 90%		5		ns
Fall Time	t_F	90% to 10%		5		ns

4.0 Application Notes

Inverting Comparator with Hysteresis

When higher levels of hysteresis are required, positive feedback can be externally added. The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (Vcc), as shown in Figure 1. When V_{IN} at the inverting input is less than V_T, the output voltage is high. The three network resistors can be represented as R1//R3 in series with R2. Equation 1 defines the high to low trip voltage (V_{T1}) .

$$V_{T1} = \frac{R2 \cdot Vcc}{(R1//R3)+R2} \quad (1)$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2//R3 in series with R1. Equation 2 define the low to high trip voltage (V_{T2}).

$$V_{T2} = \frac{(R2//R3) \cdot Vcc}{(R2//R3)+R1} \quad (2)$$

The total hysteresis provided by the network is

$$\Delta V_T = V_{T1} - V_{T2} \quad (3)$$

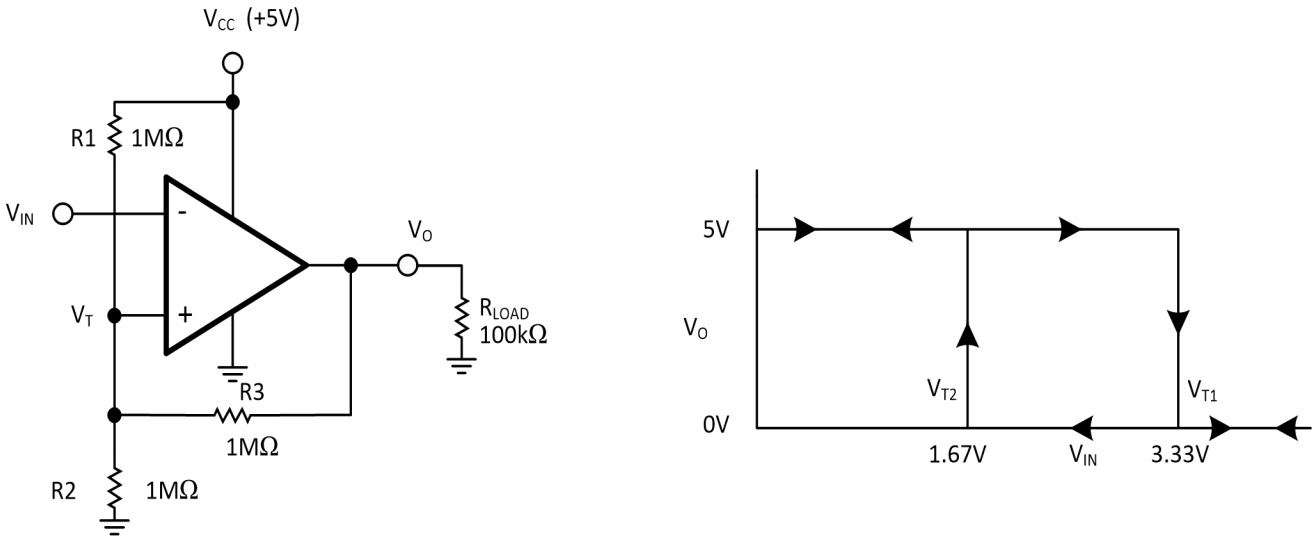


Figure 1. Inverting Configuration with Hysteresis

Non-inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 2, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Equation 4 defines the low to high trip voltage (V_{IN1}) :

$$V_{IN1} = \frac{(R1+R2)\cdot V_{REF}}{R2} \quad (4)$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2},

$$V_{IN2} = \frac{(R1+R2)\cdot V_{REF} - R1\cdot V_{CC}}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in following,

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

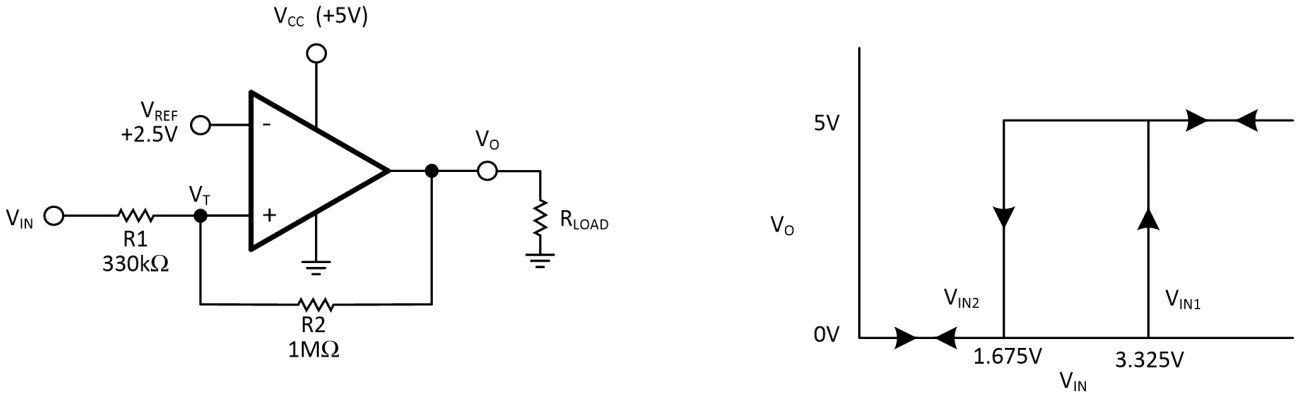


Figure 2. Non-inverting Configuration with Hysteresis

Square-Wave Oscillator

The COS3202 can be used to build a low cost square-wave oscillator as shown in Figure 3. The square-wave period is determined by the RC time constant of the capacitor (C1) and resistor (R4). The maximum frequency is limited by propagation delay of the device and the capacitance load at the output.

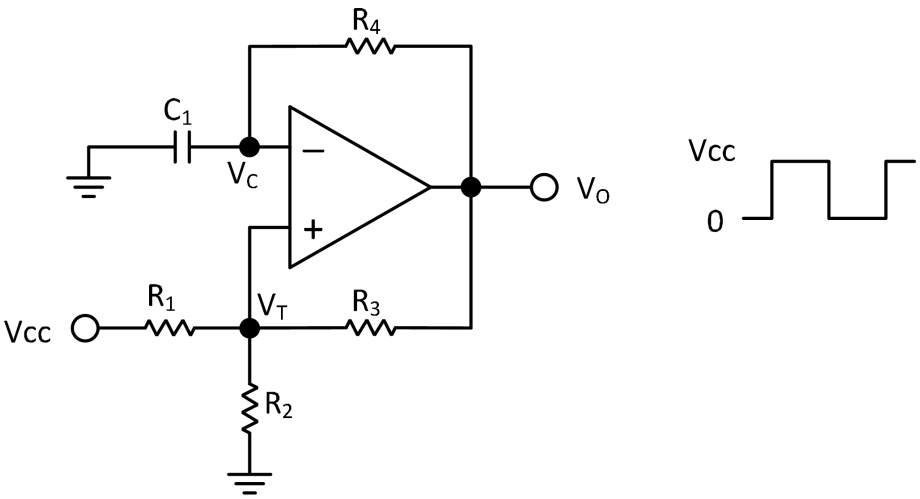


Figure 3. Square-Wave Oscillator

IR Receiver

COS3202 can be used to build a IR receiver analog front end as shown in Figure 4. R1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R2 and C1 establishes a reference voltage Vref which tracks the mean amplitude of the IR signal. The RC constant of R2 and C1 is chosen for Vref to track the received IR current fluctuation but not the actual data bit stream. The non-inverting input is connected to Vref and the output over the R3 and R4 resistor network which provides hysteresis for improved guard against spurious toggles.

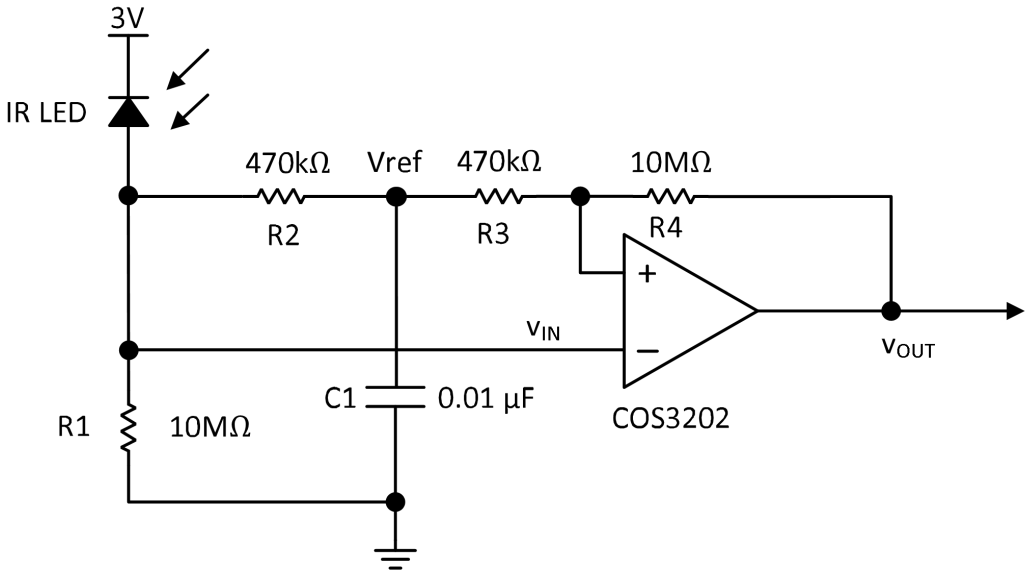


Figure 4. IR Receiver

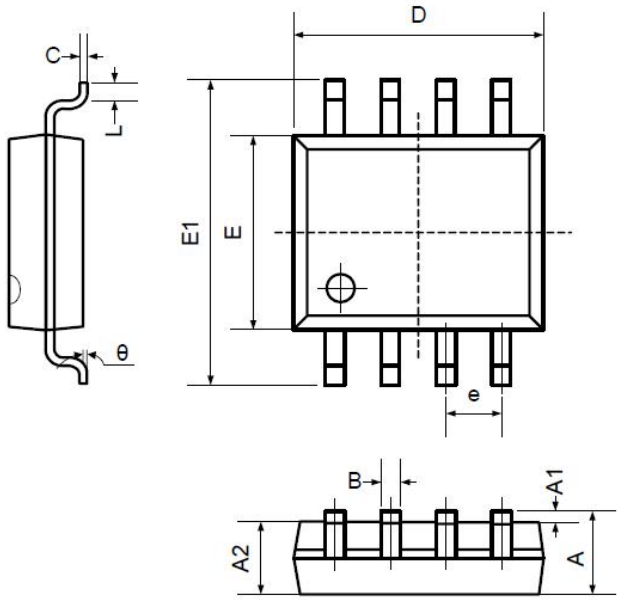
Power-Supply Bypassing and Layout

For single-supply operation, bypass the power supply V_S with a 0.1μF ceramic capacitor which should be placed close to the V_S pin. For dual-supply operation, both the positive and negative supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 2.2μF tantalum capacitor can be added for better performance.

The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance. Thus a ground plane layer is important for high speed circuit design.

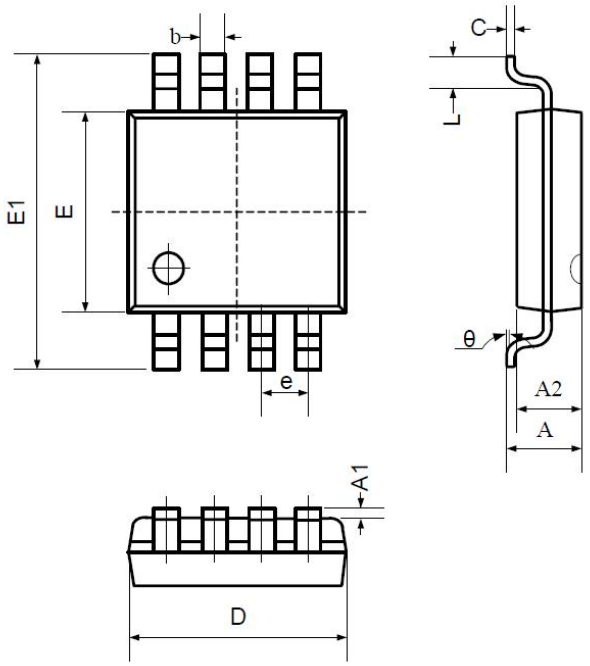
5. Package Information

5.1 SOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

5.2 MSOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
c	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°