1.8V-5.5V, 70μA, RRIO Zero-Drift, Instrumentation Amplifiers with Selectable Gain

Features

- Selectable Gain Options
  - G=20 or G=10 (COS333-20)
  - G=50 or G=30 (COS333-50)
- Shutdown Option for Power Savings
- Low offset Voltage: 10μV (typical)
- Zero Drift: 0.05μV/ºC
- Low Quiescent Current: 70μA
- Low Input Bias Current: <1pA (typical)
- Rail-to-Rail Input and Output (RRIO)
- Operates on 1.8V ~ 5.5V Supplies
- Bandwidth: 100kHz for G=10 (typical)
- Extended Temperature Ranges
  From -40°C to +125°C
- Available in MSOP8/DFN8

Applications

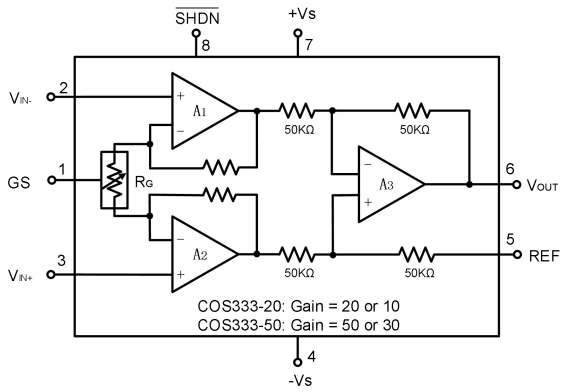
- Pressure and Temperature Sensing
- ECG and RTD Sensor Amplifiers
- Blood Glucose Monitors
- Weigh Scale
- Bridge-type Sensing Amplifiers

Rev1.1

General Description

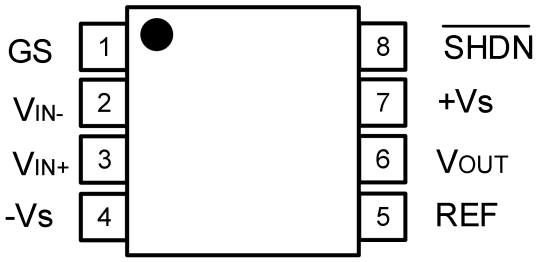
The COS333-20 and COS333-50 are gain selectable, zero-drift instrumentation amplifiers operated on 1.8 to 5.5 supplies. They don't need external precision resistors to set the gain. The gain options can be selected by toggling the gain select (GS) pin. They also have an integrated shutdown option to turn off the amplifiers when idle for additional power savings in battery powered applications.

The COS333 family uses auto-calibration technique to provide very low offset voltage (less than 125μV maximum) and near zero drift over temperature. Low quiescent supply current of 70μA and very low input bias current make the device an ideal choice for low offset, low power consumption and high impedance applications.



Block Diagram

1. Pin Configuration and Functions



COS333-20, COS333-50

Pin Functions

Pin	Name	I/O	Description	
1	GS	I	Gain setting pin:	
			COS333-20	COS333-50
			logic low: G=10 logic high: G=20 no connect: G=20	logic low: G=30 logic high: G=50 no connect: G=50
2	V_{IN-}	I	Negative input	
3	V_{IN+}	I	Positive input	
4	$-V_S$	P	Negative supply, or ground	
5	REF	I	Reference input. This Pin must be driven by low impedance or connected to ground	
6	V_{OUT}	O	Output	
7	$+V_S$	P	Positive supply	
8	$\overline{SHDN}$	I	Shutdown control: logic low - device disenabled; logic high - device enabled; no connect - device enabled.	

2. Package and Ordering Information

Gain	Model	Package	Order Number	Package Option	Marking Information
10	COS333-20	MSOP-8	COS333-20MR	Tape and Reel, 3000	COS333-20
20		DFN-8(3x3)	COS333-20FR	Tape and Reel, 3000	COS333-20
30	COS333-50	MSOP-8	COS333-50MR	Tape and Reel, 3000	COS333-50
50		DFN-8(3x3)	COS333-50FR	Tape and Reel, 3000	COS333-50

3. Product Specification

3.1 Absolute Maximum Ratings (1,2)

Parameter	Rating	Units
Power Supply: V+ to V-	6	V
Differential Input Voltage Range	±6	V
Common Mode Input voltage Range(2)	V+ to V-	V
Output Current	20	mA
Storage Temperature Range	-65 to 150	°C
Junction Temperature	150	°C
Operating Temperature Range	-40 to 125	°C
ESD Susceptibility, HBM	2000	V

(1) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

3.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance, $R_{\theta JA}$ (Juntion-to-ambient)	206 (MSOP8) 43 (DFN8-3x3)	°C/W

3.3 Recommended Operating Conditions

Parameter	Rating	Unit
DC Supply Voltage	1.8V ~ 5.5V	V
	± 0.9V ~ ± 2.75V	V
Input common-mode voltage range	-Vs ~ +Vs	V
Operating ambient temperature	-40 to +85	°C

3.4 Electrical Characteristics

(+V_S=+5V, -V_S=0V, V_{REF}=2.5V, T_A=+25°C, R_L=10 kΩ, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}			±10	±125	μV
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40 to 125°C		0.01	0.05	μV/°C
Input Bias Current	I_B	V_{CM} = V_S / 2		±0.5		pA
Input Offset Current	I_{OS}	V_{CM} = V_S / 2		±0.2		pA
Common-Mode Voltage Range	V_{CM}		-Vs		+Vs	V
Common-Mode Rejection Ratio	CMRR	V_{CM} =0.1V to 4.9V		120		dB
Output Characteristics						
Output Voltage Swing from Rail	Vhr	R_L=100kΩ		2		mV
		R_L=10kΩ		20		mV
Short-Circuit Current	I_{SR}	Sourcing		15		mA
	I_{SK}	Sinking		-15		mA
Power Supply						
Operating Voltage Range	V_S		1.8		5.5	V
			±0.9		± 2.75	V
Quiescent Current	I_Q	V_{IN}=0, EN=1, or no connect		70		μA
		EN=0			2.5	μA
Power Supply Rejection Ratio	PSRR		100	120		dB
Frequency Response						
Bandwidth, -3dB	BW	G=10 (COS333-20, GS=0)		40		kHz
		G=20 (COS333-20, GS=1)		20		
		G=30 (COS333-50, GS=0)		14		
		G=50 (COS333-50, GS=1)		8		

Dynamic Performance						
Slew Rate	SR	V_S = 5 V, V_O = 2 V step		0.22		V/μs
Amplifier Enable Time	t_{ON}			100		μs
Amplifier Disable Time	t_{OFF}			1		μs
Noise Performance						
Voltage Noise Density	e_n	f=1kHz		50		nV/ √Hz
Reference Input						
Voltage Range			-Vs		+Vs	V
Reference Input Impedance	R_{IN}			100		kΩ
Logic Control (GS, SHDN)						
Logic Low Threshold Voltage	V_{IL}				0.8	V
Logic High Threshold Voltage	V_{IH}		2.4			V

4. Application Notes

4.1 Overview

The COS333-20 and COS333-50 are gain selectable, zero-drift instrumentation amplifiers operated on 1.8 to 5.5 supplies. They don't need external precision resistors to set the gain. The gain options can be selected by toggling the gain select (GS) pin. Since the integrated resistors are precision matched with low temperature coefficient resistors, the overall gain drift would be much better in comparison to discrete implementation of the instrumentation amplifiers built using external resistors. The COS333-20 and COS333-50 also have an integrated shutdown option to turn off the amplifiers when idle for additional power savings in battery powered applications.

The COS333 family uses auto-calibration technique to provide very low offset voltage (less than 125μV maximum) and near zero drift over temperature. They have both rail-to-rail input and output range. The output voltage swing extends to within 2mV of each rail, providing the maximum output dynamic range. Low quiescent supply current of 70μA and very low input bias current make the device an ideal choice for low offset, low power consumption and high impedance applications.

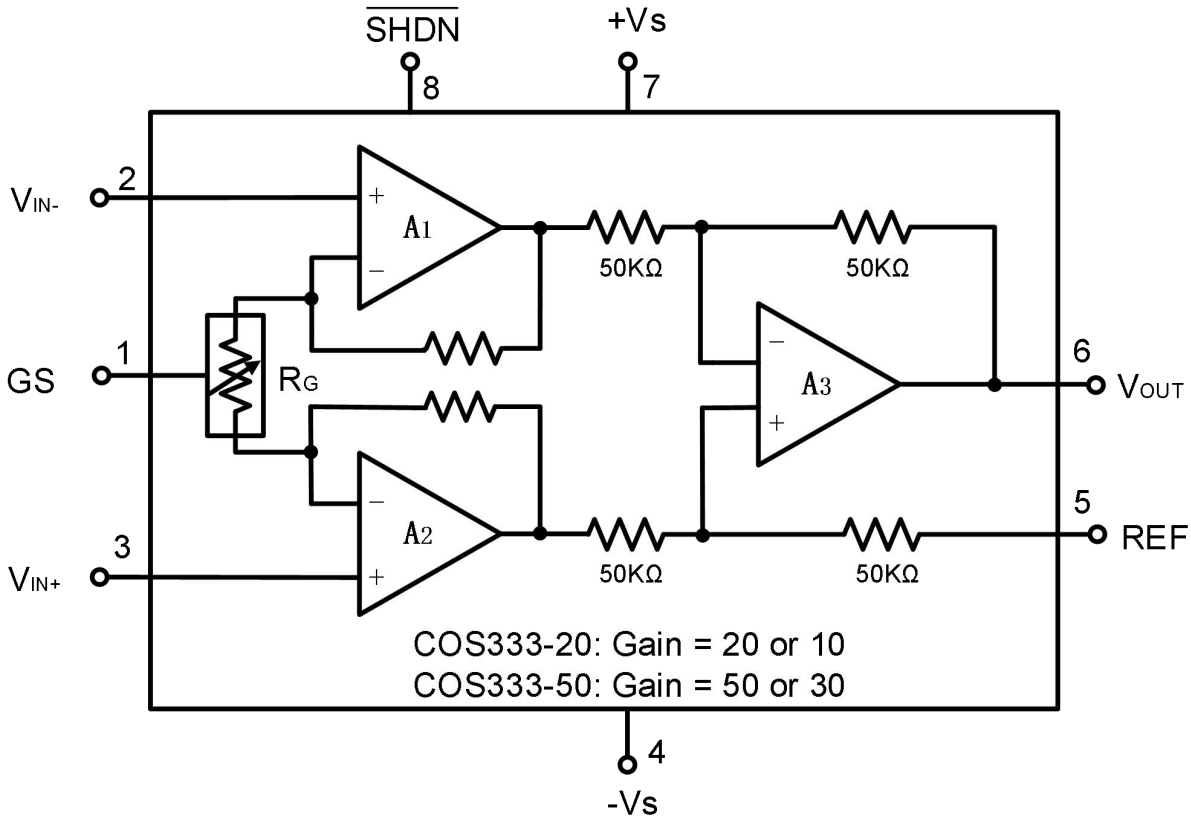


Figure 4.1 Simplified Internal Schematic

4.2 Functional Block Diagram

Figure 4.1 shows the simplified internal schematic of the COS333-20 and COS333-20. The output is referred to the REF terminal, which is normally grounded. The REF pin connection must be low-impedance to assure good common-mode rejection. A resistance of 8Ω in series with the REF pin will cause a 80dB CMRR degradation.

Table 4.1 provides how to choose different gain options across COS333-20 and COS333-50. COS333-20 has gain options of 20 or 10 and COS333-50 has gain options of 50 or 30. These gain options can be selected by toggling the gain select (GS) pin.

Table 4.1 Gain Selection Table

Device	Gain Select (GS)	Gain
COS333-20	High or No Connect	20
	Low	10
COS333-50	High or No Connect	50
	Low	30

4.3 Typical Application

Figure 4.2 illustrates a basic single-supply sensor application circuit. The output REF terminal can be connected to ground if the differential signal from the sensor is positive. V_{IN+} and V_{IN-} must both be 0.1V above ground for linear operation. A resistor (R1) in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier inputs.

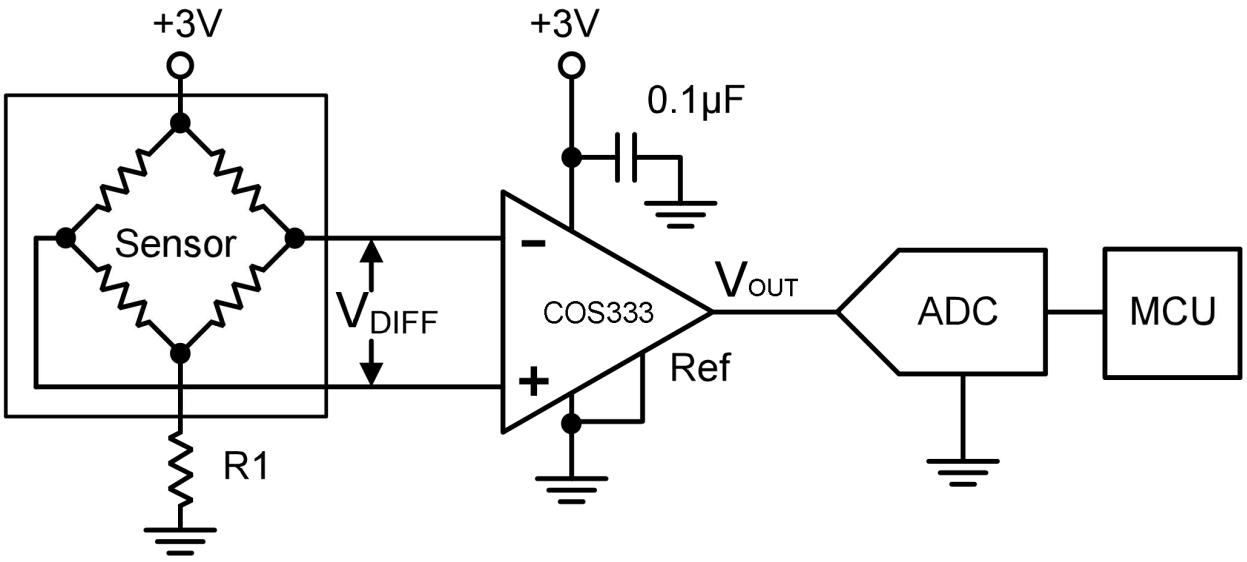


Figure 4.2 Single-Supply Bridge Amplifier

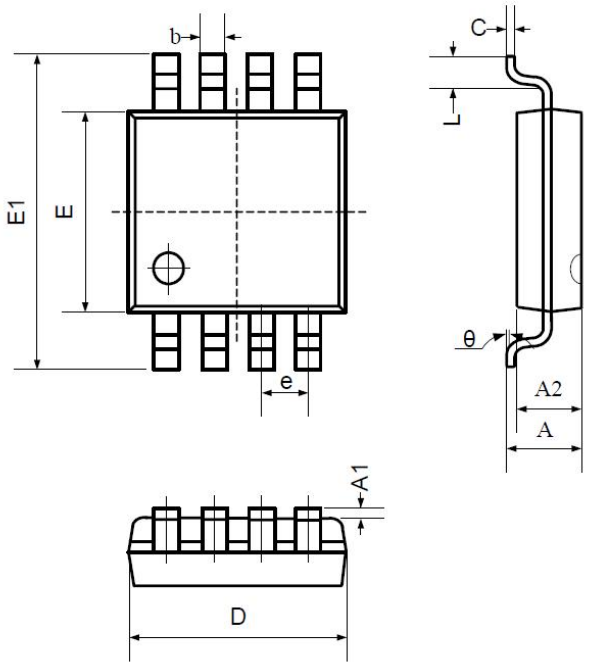
4.4 Power-Supply Bypassing and Layout

The COS333 family operates from a single +1.8V to +5.5V supply or dual ±0.9V to ±2.75V supplies. For single-supply operation, bypass the power supply +Vs with a 0.1μF ceramic capacitor which should be placed close to the +Vs pin. For dual-supply operation, both the +Vs and the -Vs supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 2.2μF tantalum capacitor can be added for better performance.

The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance. Thus a ground plane layer is important for high speed circuit design.

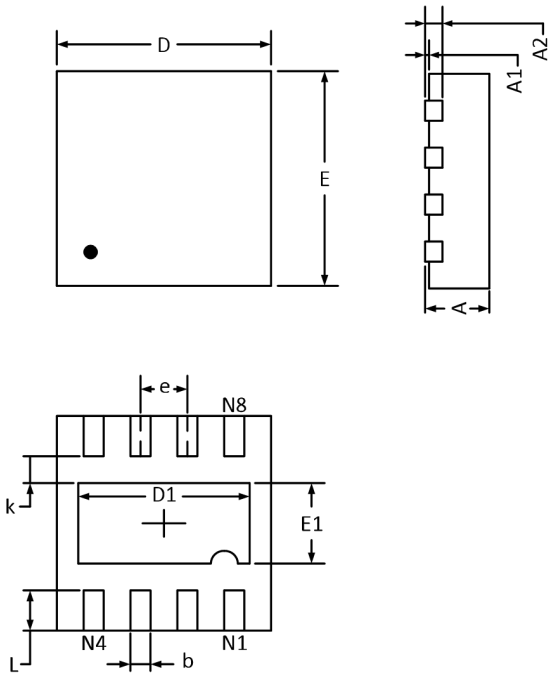
5. Package Information

5.1 MSOP-8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
c	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

5.2 DFN-8(3x3) (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	1.800	2.000	0.007	0.012
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023